UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,933,557 B2
APPLICATION NO. : 10/639073
DATED : August 23, 2005
INVENTOR(S) : Bohumil Lojek

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, line 39, insert new paragraph:

With reference to Fig. 3B, the appropriate voltages for reading, erasing, and programming the blocks of the memory array 300 are managed by a memory subsystem 330. As is known to a skilled artisan, a memory controller 340 receives memory subsystem instructions and/or control signals for programming, reading, or erasing blocks or bits of a memory device such as the memory array 300. Additionally, an input/output port 350 (I/O port) receives addresses and provides appropriate voltage levels for word line, bit line, and input/output data line selection in support of memory access operations. The I/O port 350 also provides connections for communicating data with the remainder of the system 360. By selecting word lines, bit lines, and source lines and applying appropriate voltages, the controller 340 and I/O port 350 will produce reading, erasing, and programming operations.

Column 4, line 52 through Column 5, line 13, replace paragraphs with the following paragraphs:

With reference to Fig. 4B, a cross sectional view 400 of the memory cell 310 is illustrated. The memory cell 400 is formed on a semiconductor substrate (or well) 401 of a first conductivity type, which in the exemplary embodiment is p-type. A drain implant region 402 and a source implant region 406 are implanted within an uppermost surface of the substrate 401. A buried, heavily doped implant 404 within a portion of the floating gate region is formed essentially contiguous with the source implant region 406 within the uppermost surface of the substrate 401. The implant regions 402, 404, and 406 are of a second conductivity type of a polarity opposite that of the conductivity type of the substrate 401. In a specific exemplary embodiment, the implants are n-type. The buried implant 404 is of n+ conductivity and serves as a tunneling charge source for a floating gate of the memory transistor 400. The drain implant region 402 and the buried implant 404 are spaced apart, so as to define an active region 414 in a portion of the space therebetween. Accordingly, the drain implant region 402 connects to the bitline BL_i. The source implant region 406 connects to the source line S_i.

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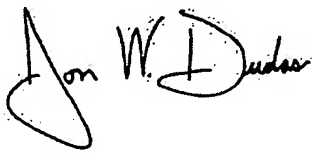
A first poly layer 410, forming the floating gate of the memory transistor 304, overlays the buried implant region 404, separated therefrom by a gate ONO layer 450. A second poly layer 408, forming a common control gate, extends continuously over the first poly layer 410 (which forms the floating gate) from the source dopant region 406 to the drain dopant region 402, overlaying both the buried implant 404 and the select transistor 302 active region 41 4. An interpoly layer 412 separates the first poly layer 410 from the second poly layer 408. The interpoly layer 412 also extends over the active region 414 and isolates the second poly layer 408 from the semiconductor substrate. The interpoly layer 412 extends continuously over the first poly layer 410 from the source dopant region 406 to the drain dopant region 402. The interpoly layer 412 may be of ONO type material. A tunnel oxide 460 of thickness 50-70 angstroms is formed in a tunnerl window region between the buried implant 404 and the floating gate 410.

Signed and Sealed this

Ninth Day of January, 2007



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